A CMOS-MEMS Test Chip for process control feedback on materials and devices properties

Carlos Ramón Báez Álvarez\textsuperscript{a}, Mónico Linares Aranda\textsuperscript{b}, Wilfrido Calleja Arriaga\textsuperscript{c}, Alfonso Torres Jacome\textsuperscript{d}

\textsuperscript{a,b,c,d} Laboratorio de Innovación en Sistemas Micro Electro Mecánicos (LI-MEMS) INAOE
Luis Enrique Erro No. 1, Sta. María Tonantzintla, P, P, Box 51, 72000, Puebla México

Author’s E-mail: \textsuperscript{a}rbaez@inaoep.mx, \textsuperscript{b}mlinares@inaoep.mx, \textsuperscript{c}wcalleja@inaoep.mx, \textsuperscript{d}atorres@inaoep.mx

\textsuperscript{a} Corresponding Author E-mail: rbaez@inaoep.mx

This work was supported by CONACyT-México under granting the scholarship 329012.

Abstract

Process monitoring and material/device property measurement at wafer level are of great importance in the development of MEMS technology. An intra-CMOS approach has been used to design the test structures which also brings the capability to be useful with any integration approach requiring different structural materials ranging from polysilicon to aluminum as well as different material thickness according to the application requirements. With the acquired data, the test chip will be useful for identifying the possible electrical and/or mechanical variations on the material properties and devices performance due to the fabrication process.

Keywords: test chip, CMOS, MEMS, test structures.
1 INTRODUCTION
A microelectromechanical system (MEMS) device usually interacts with a physical or chemical phenomenon and has an electrical input or output to correlate the performance of the device with the phenomenon. Some MEMS devices, like single transducers, must be integrated with electronics in order to perform a useful function. Other MEMS devices, like accelerometers or gyroscopes, should be integrated with electronic circuits in order to optimize their performance. For example, the increased sensitivity between the connection of pre-amplifiers and signal conditioning close to MEMS device, due to the reduction of parasitic elements (resistance, capacitance, inductance) is one of the major advantages in performance and cost. The integration of electronic circuits with mechanical structures is the real sense of the MEMS word. There are different options available to develop an integrated MEMS technology based on CMOS: 1) Pre-CMOS, where the mechanical devices are fabricated before the standard CMOS process (Smith, Montague, Sniegowski, Murray, & McWhorter, 1995); 2) Post-CMOS, where the standard CMOS process is fabricated and the mechanical structures is post-processed (Kao, Shih, Dai, & Liu, 2010); and Intra-CMOS, where an integrated process to fabricate mechanical and CMOS devices in the same foundry is used (Scheiter et al., 1998). Each one of these approaches has their own benefits and limitations and the selection of one of them is fully dependent of the application possibilities. However, from the process development viewpoint, the most important aspects to select an approach are the foundry facilities to develop, to improve or to adapt the fabrication process. To carry out the above, the integrity of the materials and the performance of the devices have to be verified, so a test chip containing different test structures it is needed. The test structures included in the design requires electrical (Bhushan & Ketchen, 2011) and/or optical (Guckel, Randazzo, & Burns, 1985), (van Drieënhuizen, Goosen, French, & Wolffenbuttel, 1993) measurements to provide the valuable data for process monitoring and feedback for the optimization of the process. This paper presents a test chip designed to evaluate the feasibility of integrating mechanical structures of different structural materials (from polysilicon to aluminum), and CMOS devices on the same wafer in an intra-CMOS approach. The main feature of this test chip design will be its utility at the wafer level during the fabrication process and with the use of minimal test equipment by using a modular pad array to facilitate the power supply and measurement of electrical and mechanical devices.

2 FABRICATION TECHNOLOGY
The fabrication process selected in this work is outlined in Fig. 1, and it is in stage of development. It requires p-type (100) wafers with 1-10 Ω-cm resistivity and 13 masks to fabricate a twin-well PBLOCOS CMOS process that has one metal and one polysilicon layer. A surface micromachining process that includes up to two layers of polysilicon as structural material also forms part of this process. The critical process steps for developing an integrated MEMS technology in which a trench will host the electromechanical devices are: 1) The proper design of alignment marks shared between the CMOS substrate area and the trench to house the mechanical structures, 2) Drive-in of the twin-wells at 1200 °C prior to the fabrication of the mechanical structures, 3) The use of a highly selective etch for removing the material outside the trench, 4) The fabrication modules required to complete the CMOS devices must be realized within the thermal budget of 1000°C to complete stress relief of the mechanical structures, 5) A reliablemetal deposition method for ensuring proper step coverage from the top of the wafer (CMOS area) to the bottom of the trench (mechanical structure area), and 6) The sacrificial etch to release the mechanical structures must guaranty the integrity of them.

This integrated MEMS technology is developed aiming at minimum influence on the performance of CMOS devices and to be compatible with different structural materials as polysilicon and aluminum, among others.
3 THE TEST CHIP

Fig. 2 shows the layout of the designed test chip. The chip size is 4.3 X 4.2 mm, and in it all the CMOS devices surround the mechanical structures. All test structures use a 2 x 5 terminal array module to facilitate the testing process at wafer level.

3.1 Design Considerations

All the mechanical structures are affected by stress and their location on the die is critical to guarantee the adequate performance of the designed device. Usually the mechanical structures are tested at a wafer level and the residual stress is produced during the fabrication process. However, the technique required to attach the die to the package (adhesive, wire bond, molding compound), may apply stress gradients to the entire wafer (Walwadkar, Farrell, Felton, & Cho, 2003), (Zhang, Park, & Judy, 2007). As the mechanical structures are stress sensitive components, it is convenient to locate them near the center of the die where the induced stresses are more uniform (Roberts et al., 2010), (Polcawich & Pulskamp, 2011). It is clear from the above that the design must include all the mechanical structures at the center of the die.

The test chip includes the following modules (highlighted in Fig. 2): A) Fabrication test structures checked during processing; B) Devices test structures (MOSFETs, capacitors, diodes); C) Process test structures (sheet resistance, contact resistance); D) Interconnection reliability test structures (continuity, sheet resistance inside the trench); E) Stress monitors (buckling structures, rotating structure); F) Micro-actuators (chevron arrays); and G) Wiring pads (to wire the micro-actuators).

Also, the test chip include diamond structures (Fernando Julian, 2009) used to determine compressive stress, and split-cross-bridge resistors (M. G. Buehler, 1978), (Martin G. Buehler & Hershey, 1986), useful in determining sheet resistance and effective line spacing. This added structures have been previously fabricated (Diaz et al., 2011), therefore their behavior is well known.

A 2 x 5 probe pad array is used in the design of the test structures to facilitate the test process by employing standard probe cards. Also, the use of a 2 x N probe pads arrangement (M. G. Buehler, n.d.), allows the test pads to be an integral part of the test structures, to avoid having common buses among the test structures in order to prevent the interference between different structures, and to obtain the highest degree of modularity. The terminal module is required mainly by the CMOS structures due to the fact that the electrical measurements can provide a relative large set of measurements in a short amount of time when are compared with the optical measurements. The test chip includes 24 CMOS pad sets. For mechanical structures only 4 pad sets are required because the other test structures are larger and require only optical inspection instead electrical testing.

4 TEST STRUCTURES DESIGN

The designed test structures are grouped into four categories: CMOS test structures, Mechanical test structures, Interconnection reliability test structures and Functional micro-actuators.

4.1 CMOS test structures

In the selected fabrication scheme it is necessary to find out the influences of the integration scheme on CMOS device performance. Standard process control monitor (PCM) structures (Bhushan & Ketchen, 2011), including capacitors, diodes, Kelvin resistors and individual CMOS devices are designed to test the device performance and process parameters after the integrated MEMS process. The CMOS devices and structures are evaluated before and after the integration, in such a way that the influences of the integration process can be evaluated.

The use of diodes as test structures will provide the reverse leakage current, the depletion capacitance and the breakdown voltage. All these parameters have different contributions according to the physical geometry.
Both the area and edge components of the current diode and the capacitance of the junction (El-Kareh & Bombard, 1986) have to be known. In order to meet the aforementioned requirement two diode structures are designed to have the same area \( A_1 = A_2 \) but differing in their perimeter by a factor of ten \( P_1 = 10P_2 \). Let \( C_A \) and \( I_A \) be the capacitance and current per unit area and \( C_P \) and \( I_P \) the capacitance and current per unit perimeter, the contributions can be obtained by the following expressions:

\[
M_P = M_1A_2 - M_2A_1 / P_1A_2 - P_2A_1 \quad (F or A/cm) \tag{1}
\]

\[
M_A = M_1P_2 - M_2P_1 / A_1P_2 - A_2P_1 \quad (F or A/cm^2) \tag{2}
\]

where \( M \) indicates the kind of measure either capacitance or current. The dimensions used in this design are one diode of 300\( \mu \)m X 300\( \mu \)m and another diode of 6000\( \mu \)m X 15\( \mu \)m. The square diode was designed and placed in standard form, however, the largest rectangular diode was coiled to the area of the 2 x 5 probe pad array, as shown in Fig 3.

The objective of include individual transistors in the test chip is to extract enough physical information for modeling the electrical behavior of the transistors. The set of transistors consist of devices with drawn gate lengths of 1.5, 3, 10 and 50 \( \mu \)m and gate widths of 50\( \mu \)m are included. The same configuration but now varying the gate width is also included for both NMOS and PMOS. One configuration is designed with common gate and bulk terminals to determine if parasitic leakage current is distorting the measurement of a particular device. The layout of an individual NMOS and an individual PMOS is shown in Fig 4.

### 4.2 Mechanical test structures

In the same way that the CMOS devices must be monitored, the mechanical structures also need test structures indicating the influence of the integrated MEMS process over the structural material. Is well known that a thermal anneal leads to lower the residual stress in the structural material (Gianchandani, Shinn, & Najafi, 1998), but the integrated scheme expose the mechanical structures to additional stress due to the deposition and etching of the different materials required by the CMOS process.

Stress gradient monitors and tensile/compressive stress monitors are the principal structures for the structural material. These mechanical test structures provide visual information about the material. All the mechanical test structures were designed to detect stress ranging between 5MPa to 100MPa for materials like polysilicon or aluminum. Nevertheless, another material like titanium, cooper or amorphous silicon can be used without modification. A maximum residual stress of 50MPa is considered suitable for suspended microstructures according to that stated in literature (Beeby, Ensell, Kraft, & White, 2003).

The test chip contains a set of structures that buckle at different strains. The residual stress can be calculated by determining which structures show a deformation. An array of 9 clamped-clamped beams with dimensions ranging from 200\( \mu \)m to 1000\( \mu \)m is used as monitor of the tensile residual stress. To estimate the stress gradient an array of 7 cantilever beams is designed with dimensions from 150\( \mu \)m to 750\( \mu \)m.

A stress monitor capable to measure both tensile and compressive strain is the rotating Vernier proposed in (van Drieënhuizen et al., 1993) which is also independent of the film thickness (Elbrecht, Storm, Catanescu, & Binder, 1997). The test structure is shown in Fig. 5 and is conveniently configured with a 180° rotated copy, in order to obtain an amplified measured displacement. The design was carried out with the expression (3) reported in (Lin, Pisano, & Howe, 1997):

\[
\varepsilon_{res} = 2 L_{sb} \delta_0 / 3 L_{ib} L_{tb} C \tag{3}
\]

\[
C = 1 - d^2 / 1 - d^3 \tag{4}
\]

\[
d = W_{ib} / L_{sb} \tag{5}
\]

where \( \varepsilon_{res} \) is the residual strain and \( \delta_0 \) is the generated displacement.
To optimize the size of the monitor structure a detailed finite element simulation was done. The Coventor Ware® software was used to simulate all the microstructures assuming a Young’s Modulus of \( E = 154 \text{ GPa} \) according to the measures obtained in (Quiñones-N et al., 2014), and Poisson’s ratio of \( \nu = 0.23 \). Fig. 6 shows the simulation of the full rotating Vernier configuration used in the test chip. The rotating Vernier was designed with a range of measurement of 5-100 MPa with a resolution (minimal recordable stress) of 5 MPa when polysilicon is used as the structural material.

### 4.3 Interconnect reliability test structures

The continuity of electrical interconnects between the mechanical structures and CMOS devices is a key component in an integrated MEMS process. The integrated scheme uses aluminum as the interconnect material. The evaluation of the metal used for interconnection is realized with a 4-points sheet resistance structures designed to measure the resistance on the bottom of the trench (Verhaar, Wei, & Sarro, 2009) as shown in Fig. 7. A track of metal crossing an array of trenches used as another test structure to validate the step coverage by the measure of the resistance of the coil. The track of metal is designed to have a resistance of 216\( R_s \) and is depicted in Fig 8.

The use of standard photolithographic methods to define the geometries inside the trench (structural material), may generate air bubbles or unwanted photoresist accumulation at the edge of the trench. This situation must be monitored by an array of simple geometries placed near the trench at different distances as shown in Fig. 9 and Fig. 10. The minimal distance to correctly define geometries will be the distance where the squares will be observed well defined at the corners.

### 4.4 Functional Micro-actuators

For functional demonstration of the integrated MEMS process, two chevron type micro-actuators were designed to verify the suitable mechanical characteristics of the structural material. The design approach for the chevron type micro-actuators was realized as described in (Baez Alvarez, Linares Aranda, Calleja Arriaga, & Molina Reyes, 2013) with the goal of have a functional design for different structural materials. Three different configurations are designed to estimate the output force of the chevron micro-actuators. The 2 x 5 terminal array is used to energize and probe the chevron type micro-actuators at wafer level. Additionally, they are interconnected outside the trench (where the micro-actuators are fabricated), to validate the interconnection. The layout of these chevron type micro-actuators is shown in Fig. 11.

An array of four chevron type micro-actuators is used to correlate the possible effects of the integrated MEMS process in the performance of micro-structures using different initial angles (0.5°, 1°, 2° and 3°). If buckling is observed in the micro-actuator array, then the integrated processes should be optimized further. Otherwise, the integrated process is compatible with the micro-structures. An example on the simulated micro-actuator, where the structure is buckled because a compressive stress produced during the fabrication process is presented in Fig. 12.

The other situation, where this configuration is useful, is when the chevron actuators are energized. If the residual strain in the structural material is tensile enough, the deflection of the arms may reach the yield strength of the material.

### 5 Conclusions

The design of a CMOS-MEMS test chip for the evaluation during both process development and fabrication is reported. The test structures provide fast and accurate optical and electrical information about the material properties to study the feasibility of the integration of CMOS devices and mechanical structures. The use of a modular array of pads is commonly used in CMOS structures however in this test chip, the modular
array is also used in mechanical structures that requires power supply. The use of the 2 x 5 probe pad array will improve the measurements to perform statistical analysis. The mechanical structures were designed to be functional with polysilicon or aluminum as structural material. Nevertheless, another similar material like titanium or amorphous silicon can be selected to fabricate the mechanical structures and the same design will be enough to measure the residual stress in the films. A wide range (5 - 100 MPa) rotating structure was designed to monitoring the strain in the film regardless the thickness of the material. The micro-actuators will provide a feedback information on the material properties according to their maximum displacement and force generated; that information will be useful for tuning simulation routines and analytical expressions. The fabrication process of the designed test chip is still in progress during the preparation of this paper.

Fig. 1. A schematic diagram summarizing the intra-CMOS process flow: a) Trench formation and P/N well drive-in. b) Microstructure fabrication. c) Complete CMOS sequence process. d) Simultaneous metallization and sacrificial etch.
Fig. 2. Layout of the CMOS-MEMS test chip.

Fig. 3. (Left) Layout of a coiled diode designed in the 2 x 5 terminal array module where the anode terminals are the coil, and the cathode terminals are the two in the bottom. (Right) Schematic cross section of p+/n diode.
Fig. 4. One subset of individual MOSFET's

Fig. 5. Schematic of the rotating structure proposed by [6]. The test beam (tb), the indicator beam (ib), and the slope beam (sb) are indicated to be used in the expression (1) for the lengths (L) and the widths (W).

Fig. 6. Finite element simulation of the rotating Vernier structure of polysilicon under a tensile stress of 50 MPa.
Fig. 7. Layout of the test structures used to determine the quality of the metal used to interconnect the CMOS and micro-structure devices.

Fig. 8. Layout of the metal coil test structure for step coverage evaluation.

Fig. 9. Layout for the photolithography quality monitor at the edge of the trench.

Fig. 10. Layout for the photolithography quality monitor at the corner of the trench.
Fig. 11. Layout for chevron type micro-actuators array.

Fig. 12. Zero current buckled chevron actuator due to residual strains

References


